DETAILED ACTION

Response to Amendment

1. Amendment filed 6/24/08 forms the basis for this Office Action. In said Amendment Applicant cancelled claims substantially amended claims 71-73, 76, 78-81, 89-91, 93-96 and 98-100, and cancelled claims 92 and 97. Applicant also filed Replacement Sheets for the Drawings of Figures 9, 11 and 12. Applicant also filed an Amendment to the Specification. Comments on Remarks submitted with said Amendment are included below under "Response to Arguments".

Drawings

2. The Replacement Drawings, containing replacements for Figures 9, 11 and 12, are herewith accepted.

Specification

3. The Amendment s to paragraphs [0070] and [0071] of the Specification are herewith accepted.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. ***Claim 98*** is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession

of the claimed invention. An "electrically conductive pillar" (lines 33-35) rather than a semiconductive pillar finds no support in the written description of the claimed invention. Its introduction thus constitutes new matter.

6. ***Claim 99*** is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention. An "electrically conductive pillar" (lines 34-36) rather than a semiconductive pillar finds no support in the written description of the claimed invention. Its introduction thus constitutes new matter.

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. ***Claims 98-99*** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The introduction of new matter as detailed above in sections 5 and 6 causes the metes and bounds of the claimed inventions to be vague and ill-defined in the absence of a written description, rendering the claims indefinite.

9. ***Claim 96*** recites the limitation "the second layer of conductive material" in lines 2-3 and 4. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. ***Claim 71*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Walker et al (6,888,750 B2), or, alternatively Walker et al (US 2001/0055838 A1), -which is the published patent application later patented as US 6,888,750 B2, in view of Yamazaki et al (6,693,044 B1) and Yamazaki et al (6,759,677 B1), henceforth referred to as "Yamazaki-1" and "Yamazaki-2", respectively (all previously cited), Aoki et al (US 4,768,076; made of record by applicant in IDS) and Rodder (US 5,324,961). N.B.: while the Figures in the patent to Walker et al are of a substantially higher quality of reproduction, no essential difference exists in the details nor in their numbering. Columns refer to the patent to Walker et al, paragraph numbers to the corresponding published publication.

Walker et al teach a computer system (col. 1) (e.g., logic circuits (Figures 12-14) together with the nonvolatile memory array (see "Field of Invention") constitute a computer system) with stacking according to the embodiment of Figure 9 (col. 14, l. 61-67 or [0096]) comprising: a signal source capable to provide a data signal (from word line 445; col. 17, lines 60-65 or [0112]); and an inverter 443 coupled with the signal source (col. 17, l. 45-46 or [0111]), capable to invert the data signal and output the

inverted signal (through bit lines 447); the inverter including (Figure 9, i.e., "CMOS array" "in pillar or self-aligned TFT configurations"):

a substrate 413/415 comprising semiconductor material (Figure 11; see col. 15, l. 28 – 36 or [0100]) comprising at least silicon (col. 1,, l. 6-8);

a first transistor (PMOS TFT: see col. 14, l. 66 – col. 15, l. 2 or [0096] on the inclusion of both options, PMOS with NMOS stacked thereon or *vice versa*) (with gate 243; Figure 9, and col. 11, l. 28-30 or [0072]) supported by the substrate, the first transistor comprising a first gate 243 (Figure 9 and col. 11, l. 28-30 or [0072]) and first active region 219: Figure 9 and col. 11, l. 24-26 or [0072]) proximate the first gate; the first active region including a first channel region (219 = region between neighboring s/d regions 217) and a pair of first source/drain regions 217 (col. 11, l. 24-26 or [0072]); at least a portion of the first active region being within the substrate (Figure 9), the first transistor being a PFET (i.e., a PMOS TFT: see col. 14, l. 66 – col. 15, 2 or [0096] on the inclusion of both options, PMOS with NMOS stacked thereon or *vice versa*) and the first source/drain regions accordingly being p-doped regions; the first gate being substantially non-overlapping with respect to the first source/drain regions (because the embodiment of Figure 9 has gates 243 and 217 in a substantially non-overlapping configuration as evident from Figure 9);

an insulative material 203 (col. 11, l. 42-44 or [0073]) over at least a portion of the first transistor (Fig.9);

a second transistor over the material layer and comprising a second gate 243 (col. 11, l. 2-8 or [0070]) and a pair of source and drain regions 217 (col. 11, l. 24-26 or

[0071]), the second transistor being an NFET (NMOS TFT)) (Figure 9 and col. 14, l. 66 – col. 12, l. 2) or [0096]) and the second source/drain regions accordingly being n-type doped regions (loc.cit.); the second gate being directly over the first gate (Figure 9: 243 being directly over each other); the second gate being substantially non-overlapping with respect to the second source/drain regions (because the embodiment of Figure 9 has gates 243 and 217 in a substantially non-overlapping configuration as evident from Figure 9);

the first and second gates being electrically connected to one another (see Figures 12-14 and col. 16, l. 58-60 or [0108]), and being in electrical connection with the signal source 471 (Figure 14); and

one of the first source/drain regions being electrically connected to one of the second source/drain regions and being in electrical connection with the output (Figure 14).

Although Walker et al do not specifically teach the structure of the specific embodiment of Figure 9 to comprising also germanium, it would have been obvious to comprise germanium in view of the teaching by Walker et al in a non-volatile memory array (Figure 1 and cols. 2-3), hence analogous art, that germanium addition may be advantageously used as a seed for the crystallization of amorphous silicon (comprising silicon and germanium (see col. 3, l. 28-41)). *Motivation* for inclusion of the teaching by Walker et al also for the CMOS TFT array as described above derives from the resulting advantage of thus achieving polysilicon mobility through efficient manufacturing from a relatively cheap source material (amorphous silicon).

Walker et al do not necessarily teach the limitation "a first layer of semiconductive material over the insulative material; a second layer of semiconductive material over the first layer, the second layer of semiconductive material physically contacting the first layer of semiconductive material, and the second layer of semiconductive material being compositionally different from the first layer of semiconductive material", i.e., lines 13-17 of claim 71.

However, it would have been obvious to include said further limitation in view of Yamazaki-1, who, in a patent on TFTs (thin film transistors) (cols. 1-2), hence analogous art (see Walker et al, cols. 12-14), teach in their Embodiment 2 (cols. 8-10) the TFT to be supported by a first layer of semiconductive material 202 (see Figures 2, col. 8, l. 39-49 and col. 9, l. 1-30) over insulative material 200 (loc.cit.) and a second layer of semiconductive material 204 (col. 9, l. 35-67) physically contacting the first layer of semiconductive material (see Figure 2E and col. 9, l. 35-39), and the second layer of semiconductive material being compositionally different from the first layer of semiconductive material (nickel does exist in 202, and the concentration of nickel, in expression of contrast according to Yamazaki-1, exists hardly in 204: see col. 10, l. 1-5).

Motivation to include the teaching by Yamazaki-1 in the invention by Walker et al derives from the improved device characteristics by virtue of the strongly reduced nickel content of the second semiconductive material layer, which supports the active region of the TFT (col. 10, l. 1-19, especially l. 1-5).

Although Yamazaki-1 appears to specifically only teach the application of his teaching to silicon semiconductive material for the channel supporting layers,

Yamazaki_2 actually teach the application of nickel as a catalyst for crystallization through anneal and the use of laser annealing not only for silicon but equally for silicon-germanium (see "Background of the Invention" for the teaching of the reason why application is extended to silicon-germanium, i.e., increased mobility: col. 1, l. 5-65; and see col. 4, l. 24-28), and hence provides testimony of both the *combinability* and the motivation to include application also to silicon-germanium as the basic material for the semiconductor films.

N.B.: Drawings and pictures can anticipate claims if they clearly show the structure which is claimed. *In re Mraz, 455 F.2d 1069, 173 USPQ 25 (CCPA 1972).*

Walker et al do not necessarily teach the limitation "a vertically extending electrically conductive pillar in physical contact with one of the first source / drain regions and also in physical contact with the first layer of semiconductor material". However, in view of Aoki et al, who, in a patent on crystalline CMOS devices with stacked transistors (title, abstract and Background), hence analogous art, it would have been obvious to teach a vertically extending, aluminum pillar 74 in physical contact with one of the first source drain regions 65 and also in physical contact with the first semiconductor ('n-type high-impurity) layer 72 above the insulating layer(s) 67 and 73 separating the two transistors (with gates 63 and 70, resp.) (see Figure 5 and col. 3, l. 7 -66), to serve as interconnect between the transistors in the CMOS. Motivation to include the teaching by Aoki et al in the invention by Walker et al derives at least from the desirability as is known by those of ordinary skill in the art to have as short and as

complete a connection between the transistors in any CMOS TFT array including the one by Walker et al (CMOS array in pillar or self-aligned configurations).
Although Aoki et al do not teach said pillar to be doped semiconductive rather than a conductive Rodder, in a patent on a stacked CMOS SRAM cell (title, abstract and "Background of the Invention"), hence analogous art, teaches semiconductor material selection for interconnects 16, 30 (col. 2, l. 54 – col. 3, l. 10), from which teaching one of ordinary skill in the art would conclude that interconnects in stacked CMOS devices is an acceptable embodiment with predictable results. Evidently, the doping type should correspond to the conductivity type of the parts top be connected, which in the case of Walker is p-type. The claim would have been obvious because one of ordinary skill has good reason to pursue the known options within his or her technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense. See MPEP 2141, section III, rationale E. In this regard, applicant is additionally reminded that Applicant is reminded in this regard that it has been held that mere selection of known materials generally understood to be suitable to make a device, the selection of the particular material being on the basis of suitability for the intended use, would be entirely obvious. See MPEP 2144.07.

3. ***Claims 72-73, 76, 80-81, 89-91 and 93*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Walker et al, Yamazaki_1, Yamazaki_2, Aoki et al and Rodder as applied to claim 71 above, and further in view of Bulsara et al (US 2003/0030091 A1) (previously cited).

As detailed above, claim 71 is unpatentable over Walker et al in view of Yamazaki-1, Yamazaki-2, Aoki et al and Rodder. None necessarily teach the further limitations defined by claims 72, 73, 80 or 81.

However, it would have been obvious to include said limitations in view of the teaching as prior art by Bulsara et al that relaxed silicon-germanium including a strained layer 18 formed of silicon ([0036], hence claim 73 is also met and, being a SiGe layer ([0036], claim 76 is also met) (i.e., layer with strained lattice, hence inherently crystalline in addition to being strained) and a relaxed underlying silicon-germanium (hence claim 80 also met) crystalline layer 14 ([0035]) (with from 20 to 90 % germanium, hence claim 81 is met because there necessarily is one % value contained in the claimed range) directly applied on a graded silicon-germanium (SiGe) layer 12 (loc.cit.) (i.e., on top of a crystalline silicon-containing layer (inherently crystalline, because without being crystalline here cannot be a grading of the lattice constant (see [0003]) so as to produce field effect transistors (FETs) with increased channel mobility, hence improved device speed (loc.cit.) Implementation of the teaching for both the NFET and the PFET by Walker et al necessarily leads to the claimed device because the source/drain regions in Walker et al extend throughout the entire silicon substrate, being members of a poly bit line 333 (see Figure 10A, and see column 13, lines 20-28 or [0085]).

Motivation to include the teaching by Bulsara et al in the invention by Walker et al derives at least from the resulting improvement in device speed as taught by Bulsara (loc.cit.).

On claim 89: in Walker et al (Figure 9) the first channel region 219 is between the source/drain regions 217; the first gate 243 is above the first channel region; and the width of the first gate with respect to a cross sectional view of the inverter is substantially the same as the width of the first channel region 219 with respect to the cross sectional view (said cross-sectional view being defined by the source-drain connection and normal to the upper main surface of source/drain regions). (See Figure 9).

On claim 90: in Walker (Figure 9) the first gate 243 is neither above nor below the first source/drain regions 217 and the second gate 243 is neither above nor below the second source/drain regions 217 (Figure 9).

On claims 91 and 93: in the combined invention the inverter further comprises a vertically extending pillar in electrical contact with one of the first source/drain regions and also in electrical contact with 0the first (horizontal) layer of semiconductor material (202 in Yamazaki-1) through electrical contact with the I/O/output layer (source/drain electrode) 116 (in Walker et al) (Fig. 8 and col. 9, l. 51 – col. 10, l. 52 or [0065]), because the first semiconductor layer is in electrical contact with the source/drain electrode of the second transistor (an oxide layer on the upper main surface of 202 is removed (Yamazaki-1, col. 9, l. 35+) through 204.

4. ***Claims 78 and 79*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Walker et al, Yamazaki-1, Yamazaki-2, Aoki et al, Rodder and Bulsara et al as applied to claim 72 above, and further in view of Hsu et al (6,793,731 B1) (previously cited).

As detailed above, claim 72 is unpatentable over Walker et al in view of Yamazaki-1, Yamazaki-2, Aoki et al and Rodder, and Bulsara et al, none necessarily teaching the further limitation defined by claim 78 or claim 79. However, said limitations would have been obvious over Hsu et al, who teach as prior art polycrystalline SiGe (cols. 1-2), while teaching as improvement thereof single-crystal relaxed SiGe free of defects (abstract and col. 2, l. 65 – col. 5, l. 65). It has been held that mere selection of known materials generally understood to be suitable to make a device, the selection of the particular material being on the basis of suitability for the intended use, would be entirely obvious. In re Leshin 125 USPQ 416.

5. ***Claims 94-95*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Walker et al (6,888,750 B2), Yamazaki et al (6,693,044 B1), Yamazaki et al (6,759,677 B1), henceforth referred to as "Yamazaki-1" and "Yamazaki-2", respectively (previously cited), Aoki et al (US 4,768,076; made of record by applicant in IDS) and Rodder as applied to claim 71 above, and further in view of Kadosh et al (US 6,259,118 B1).

As detailed above, claim 71 is unpatentable over Walker et al in view of Yamazaki_1 and '-2, Aoki et al and Rodder. None of these references necessarily teach the pillar to contact the first layer of semiconductive material directly under one of the second source/drain regions, although in the combined invention all other limitations defined by claim 96 are met. However, it has long been recognized that the vertical interconnect in the form of a pillar connecting a lower transistor's source drain region with the semiconductor layer of the upper transistor in an essentially straight manner, thus connecting the upper semiconductor layer directly under said source/drain region

of the second transistor; See, e.g., Kadosh et al, who, in a patent on a stacked transistor arrangement (title, abstract), hence analogous art, teach, so as to minimize propagation delay conductors to brings output and achieve high-speed interconnection (col. 2, l. 58 - col. 3, l. 10) by interconnection between functions at different vertical levels arranged along relatively short vertical electrical connections (col. 3, l. 64 –col. 4, l. 10) (see Figure 13 for said vertical connection or pillar 61 connecting the semiconductor layer 44 of the upper transistor 52 (Figs. 8 and 13) with source drain region 28 of the lower transistor 14 (Figure 13) (col. 10, l. 27-48). One of ordinary skill in the art would have recognized the teaching by Kadosh et al to be advantageous to all connections between transistors in inverters such as Walker et al, speed being a generic advantage in the art. Motivation directly derives from the resulting higher speed as taught by Kadosh et al. With regard to claim 95, when in the combined invention a semiconductive material is selected following Rodder, it is noted, and examiner takes official notice, that, a process using a mask for the doping of the interconnect as described by Rodder (col. 3, l. 1-3) inherently leads to different regions with a different ion doping concentration by virtue of the inherent slopes in concentration achieved by ion implantation.

6. ***Claim 96*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Walker et al (6,888,750 B2), Yamazaki et al (6,693,044 B1), Yamazaki et al (6,759,677 B1), henceforth referred to as "Yamazaki-1" and "Yamazaki-2", respectively (all previously cited), Aoki et al (US 4,768,076; made of record by applicant in IDS) and Rodder as applied to claim 71 above, and further in view of Lee et al (US 2002/0058365 A1). As

detailed above, claim 71 is unpatentable over Walker et al in view of Yamazaki-1, Yamazaki-2, Aoki et al and Rodder.

N.B.: The rejection is provided subject to the noted indefiniteness under 35 USC 112, 2nd paragraph, as detailed above, whereby it is assumed that "conductive" is to be interpreted as "semiconductive" so as to conform with the requirement of antecedent basis.

None of the above references teach the further limitation defined by claim 96. However, it would have been obvious to include said further limitation in view of Lee et al, who, in a patent on a method of manufacturing a thin film transistor, hence analogous art, teach the channel region of said TFT to be formed within a single crystal region 13' so as to increase device characteristics, especially mobility (see [0005] and [0082]-[0083]). *Motivation* to include the teaching by Lee et al in the device by Walker directly flows from the increase in mobility and hence device speed thus achieved as taught by Lee et al (loc.cit.).

7. ***Claims 98-99*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Walker et al (6,888,750 B2) or US 2001/0055838 A1) in view of Yamazaki et al (6,693,044 B1) and Yamazaki et al (6,759,677 B1), henceforth referred to as "Yamazaki-1" and "Yamazaki-2", respectively (all previously cited) and Aoki et al (US 4,768,076; made of record by applicant in IDS).

Walker et al teach a computer system (col. 1) (e.g., logic circuits (Figures 12-14) together with the nonvolatile memory array (see "Field of Invention") constitute a computer system) with stacking according to the embodiment of Figure 9 (col. 14, l. 61-

67 or [0096]) comprising: a signal source capable to provide a data signal (from word line 445; col. 17, lines 60-65 or [0112]); and an inverter 443 coupled with the signal source (col. 17, l. 45-46 or [0111]), capable to invert the data signal and output the inverted signal (through bit lines 447); the inverter including (Figure 9, i.e., "CMOS array" "in pillar or self-aligned TFT configurations"):

a substrate 413/415 comprising semiconductor material (Figure 11; see col. 15, l. 28 – 36 or [0100]) comprising at least silicon (col. 1,, l. 6-8);

a first transistor (PMOS TFT: see col. 14, l. 66 – col. 15, l. 2 or [0096] on the inclusion of both options, PMOS with NMOS stacked thereon or *vice versa*) (with gate 243; Figure 9, and col. 11, l. 28-30 or [0072]) supported by the substrate, the first transistor comprising a first gate 243 (Figure 9 and col. 11, l. 28-30 or [0072]) and first active region 219: Figure 9 and col. 11, l. 24-26 or [0072]) proximate the first gate; the first active region including a first channel region (219 = region between neighboring s/d regions 217) and a pair of first source/drain regions 217 (col. 11, l. 24-26 or [0072]); at least a portion of the first active region being within the substrate (Figure 9), the first transistor being a PFET (i.e., a PMOS TFT: see col. 14, l. 66 – col. 15, 2 or [0096] on the inclusion of both options, PMOS with NMOS stacked thereon or *vice versa*) and the first source/drain regions accordingly being p-doped regions; the first gate being substantially non-overlapping with respect to the first source/drain regions (because the embodiment of Figure 9 has gates 243 and 217 in a substantially non-overlapping configuration as evident from Figure 9);

an insulative material 203 (col. 11, l. 42-44 or [0073]) over at least a portion of the first transistor (Fig.9);

a second transistor over the material layer and comprising a second gate 243 (col. 11, l. 2-8 or [0070]) and a pair of source and drain regions 217 (col. 11, l. 24-26 or [0071]), the second transistor being an NFET (NMOS TFT)) (Figure 9 and col. 14, l. 66 – col. 12, l. 2) or [0096]) and the second source/drain regions accordingly being n-type doped regions (loc.cit.); the second gate being directly over the first gate (Figure 9: 243 being directly over each other); the second gate being substantially non-overlapping with respect to the second source/drain regions (because the embodiment of Figure 9 has gates 243 and 217 in a substantially non-overlapping configuration as evident from Figure 9);

the first and second gates being electrically connected to one another (see Figures 12-14 and col. 16, l. 58-60 or [0108]), and being in electrical connection with the signal source 471 (Figure 14); and

one of the first source/drain regions being electrically connected to one of the second source/drain regions and being in electrical connection with the output (Figure 14).

Although Walker et al do not specifically teach the structure of the specific embodiment of Figure 9 to comprising also germanium, it would have been obvious to comprise germanium in view of the teaching by Walker et al in a non-volatile memory array (Figure 1 and cols. 2-3), hence analogous art, that germanium addition may be advantageously used as a seed for the crystallization of amorphous silicon (comprising

silicon and germanium (see col. 3, l. 28-41)). *Motivation* for inclusion of the teaching by Walker et al also for the CMOS TFT array as described above derives from the resulting advantage of thus achieving polysilicon mobility through efficient manufacturing from a relatively cheap source material (amorphous silicon).

Walker et al do not necessarily teach the limitation "a first layer of semiconductive material over the insulative material; a second layer of semiconductive material over the first layer, the second layer of semiconductive material physically contacting the first layer of semiconductive material, and the second layer of semiconductive material being compositionally different from the first layer of semiconductive material", i.e., lines 13-17 of claim 71.

However, it would have been obvious to include said further limitation in view of Yamazaki-1, who, in a patent on TFTs (thin film transistors) (cols. 1-2), hence analogous art (see Walker et al, cols. 12-14), teach in their Embodiment 2 (cols. 8-10) the TFT to be supported by a first layer of semiconductive material 202 (see Figures 2, col. 8, l. 39-49 and col. 9, l. 1-30) over insulative material 200 (loc.cit.) and a second layer of semiconductive material 204 (col. 9, l. 35-67) physically contacting the first layer of semiconductive material (see Figure 2E and col. 9, l. 35-39), and the second layer of semiconductive material being compositionally different from the first layer of semiconductive material (nickel does exist in 202, and the concentration of nickel, in expression of contrast according to Yamazaki-1, exists hardly in 204: see col. 10, l. 1-5).

Motivation to include the teaching by Yamazaki-1 in the invention by Walker et al derives from the improved device characteristics by virtue of the strongly reduced nickel

content of the second semiconductive material layer, which supports the active region of the TFT (col. 10, l. 1-19, especially l. 1-5).

Although Yamazaki-1 appears to specifically only teach the application of his teaching to silicon semiconductive material for the channel supporting layers, Yamazaki_2 actually teach the application of nickel as a catalyst for crystallization through anneal and the use of laser annealing not only for silicon but equally for silicon-germanium (see "Background of the Invention" for the teaching of the reason why application is extended to silicon-germanium, i.e., increased mobility: col. 1, l. 5-65; and see col. 4, l. 24-28), and hence provides testimony of both the *combinability* and the motivation to include application also to silicon-germanium as the basic material for the semiconductor films.

N.B.: Drawings and pictures can anticipate claims if they clearly show the structure which is claimed. *In re Mraz, 455 F.2d 1069, 173 USPQ 25 (CCPA 1972).*

Walker et al do not necessarily teach the limitation "a vertically extending electrically conductive pillar in physical contact with one of the first source / drain regions and also in physical contact with the first layer of semiconductor material". However, it would have been obvious to include said limitation in view of Aoki et al, who, in a patent on crystalline CMOS devices with stacked transistors (title, abstract and Background), hence analogous art, teach a vertically extending, electrically conductive (aluminum) pillar 74 in physical contact with one of the first source drain regions 65 and also in physical contact with the first semiconductor ('n-type high-impurity) layer 72 above the insulating layer(s) 67 and 73 separating the two transistors (with gates 63

and 70, resp.) (see Figure 5 and col. 3, l. 7 -66), so as to establish electrical contact terminal Vout between the common source/drain region in the CMOS device. Motivation to include the teaching by Aoki et al in the invention by Walker et al derives at least from the desirability as is known by those of ordinary skill in the art to have as short and as complete a connection between the source / drain regions forming the common source/drain terminal in any CMOS TFT array including the one by Walker et al (CMOS array in pillar or self-aligned configurations).

Regarding claim 99: examiner takes official notice that a consistent interchange of conductivity types from a specific selection of n-type and p-type conductivities of the first and second transistor is generally considered by those of ordinary skill in the semiconductor art to be entirely obvious.

8. ***Claim 100*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Walker et al ((6,888750 B2) or US 2001/0055838 A1) in view of Yamazaki et al (6,693,044 B1) and Yamazaki et al (6,759,677 B1), henceforth referred to as "Yamazaki-1" and "Yamazaki-2", respectively (all previously cited) and Lee et al (US 2002/0058365 A1).

Walker et al teach a computer system (col. 1) (e.g., logic circuits (Figures 12-14) together with the nonvolatile memory array (see "Field of Invention") constitute a computer system) with stacking according to the embodiment of Figure 9 (col. 14, l. 61-67) or [0096]) comprising: a signal source capable to provide a data signal (from word line 445; col. 17, lines 60-65 or [0112]); and an inverter 443 coupled with the signal source (col. 17, l. 45-46 or [0111]), capable to invert the data signal and output the

inverted signal (through bit lines 447); the inverter including (Figure 9, i.e., "CMOS array" "in pillar or self-aligned TFT configurations"):

a substrate 413/415 comprising semiconductor material (Figure 11; see col. 15, l. 28 – 36 or [0100]) comprising at least silicon (col. 1,, l. 6-8);

a first transistor (PMOS TFT: see col. 14, l. 66 – col. 15, l. 2 or [0096]) on the inclusion of both options, PMOS with NMOS stacked thereon or *vice versa*) (with gate 243; Figure 9, and col. 11, l. 28-30) supported by the substrate, the first transistor comprising a first gate 243 (Figure 9 and col. 11, l. 28-30 or [0072]) and first active region 219: Figure 9 and col. 11, l. 24-26 or [0072]) proximate the first gate; the first active region including a first channel region (219 = region between neighboring s/d regions 217) and a pair of first source/drain regions 217 (col. 11, l. 24-26 or [0072]); at least a portion of the first active region being within the substrate (Figure 9), the first transistor being a PFET (i.e., a PMOS TFT: see col. 14, l. 66 – col. 15, 2 or [0096] on the inclusion of both options, PMOS with NMOS stacked thereon or *vice versa*) and the first source/drain regions accordingly being p-doped regions; the first gate being substantially non-overlapping with respect to the first source/drain regions (because the embodiment of Figure 9 has gates 243 and 217 in a substantially non-overlapping configuration as evident from Figure 9);

an insulative material 203 (col. 11, l. 42-44 or [0073]) over at least a portion of the first transistor (Fig.9);

a second transistor over the material layer and comprising a second gate 243 (col. 11, l. 2-8 or [0070]) and a pair of source and drain regions 217 (col. 11, l. 24-26 or

[0071]), the second transistor being an NFET (NMOS TFT)) (Figure 9 and col. 14, l. 66 – col. 12, l. 2 or [0096]) and the second source/drain regions accordingly being n-type doped regions (loc.cit.); the second gate being directly over the first gate (Figure 9: 243 being directly over each other); the second gate being substantially non-overlapping with respect to the second source/drain regions (because the embodiment of Figure 9 has gates 243 and 217 in a substantially non-overlapping configuration as evident from Figure 9);

the first and second gates being electrically connected to one another (see Figures 12-14 and col. 16, l. 58-60 or [0108]), and being in electrical connection with the signal source 471 (Figure 14); and

one of the first source/drain regions being electrically connected to one of the second source/drain regions and being in electrical connection with the output (Figure 14).

Although Walker et al do not specifically teach the structure of the specific embodiment of Figure 9 to comprising also germanium, it would have been obvious to comprise germanium in view of the teaching by Walker et al in a non-volatile memory array (Figure 1 and cols. 2-3), hence analogous art, that germanium addition may be advantageously used as a seed for the crystallization of amorphous silicon (comprising silicon and germanium (see col. 3, l. 28-41)). *Motivation* for inclusion of the teaching by Walker et al also for the CMOS TFT array as described above derives from the resulting advantage of thus achieving polysilicon mobility through efficient manufacturing from a relatively cheap source material (amorphous silicon).

Walker et al do not necessarily teach the limitation "a first layer of semiconductive material over the insulative material; a second layer of semiconductive material over the first layer, the second layer of semiconductive material physically contacting the first layer of semiconductive material, and the second layer of semiconductive material being compositionally different from the first layer of semiconductive material", i.e., lines 13-17 of claim 71.

However, it would have been obvious to include said further limitation in view of Yamazaki-1, who, in a patent on TFTs (thin film transistors) (cols. 1-2), hence analogous art (see Walker et al, cols. 12-14), teach in their Embodiment 2 (cols. 8-10) the TFT to be supported by a first layer of semiconductive material 202 (see Figures 2, col. 8, l. 39-49 and col. 9, l. 1-30) over insulative material 200 (loc.cit.) and a second layer of semiconductive material 204 (col. 9, l. 35-67) physically contacting the first layer of semiconductive material (see Figure 2E and col. 9, l. 35-39), and the second layer of semiconductive material being compositionally different from the first layer of semiconductive material (nickel does exist in 202, and the concentration of nickel, in expression of contrast according to Yamazaki-1, exists hardly in 204: see col. 10, l. 1-5).

Motivation to include the teaching by Yamazaki-1 in the invention by Walker et al derives from the improved device characteristics by virtue of the strongly reduced nickel content of the second semiconductive material layer, which supports the active region of the TFT (col. 10, l. 1-19, especially l. 1-5).

Although Yamazaki-1 appears to specifically only teach the application of his teaching to silicon semiconductive material for the channel supporting layers,

Yamazaki_2 actually teach the application of nickel as a catalyst for crystallization through anneal and the use of laser annealing not only for silicon but equally for silicon-germanium (see "Background of the Invention" for the teaching of the reason why application is extended to silicon-germanium, i.e., increased mobility: col. 1, l. 5-65; and see col. 4, l. 24-28), and hence provides testimony of both the *combinability* and the motivation to include application also to silicon-germanium as the basic material for the semiconductor films.

N.B.: Drawings and pictures can anticipate claims if they clearly show the structure which is claimed. *In re Mraz, 455 F.2d 1069, 173 USPQ 25 (CCPA 1972).*

Finally, Yamazaki_1, although teaching said second layer of semiconductive material to be a crystalline layer (col. 9, l. 65+), do not necessarily teach the limitation that said second channel layer to be "within a single crystal" of said second layer; however, it would have been obvious to include said limitation in view of Lee et al, who, in a patent on a method of manufacturing a thin film transistor, hence analogous art, teach the channel region of said TFT to be formed within a single crystal region 13' so as to increase device characteristics, especially mobility (see [0005] and [0082]-[0083]). Motivation to include the teaching by Lee et al in the device by Walker directly flows from the increase in mobility and hence device speed thus achieved as taught by Lee et al.

Response to Arguments

9. Applicant's arguments filed 6/24/08 have been fully considered but they are not in every respect persuasive. Although the objections and rejections under 35 U.S.C. 112

as well as the double patenting rejections previously made of record were successfully overcome, further consideration of the claims as amended have revealed that the prior art as applied can be applied also to the claims that stand rejected and also should be applied to those claims for which no art rejections had previously been applied, if needed with additional art supplementing the rejection(s), with regrets by examiner. Accordingly, the present office action is made non-final. An earlier publication US 2001/0055838 A1 of the application by Walker later patented as the previously applied US 6,888, 750 B2 patent is also included as alternative over the rejection by Walker et al so as to forewarn applicant not to swear behind the date of the Walker patent, although the printing quality of several Drawings in the published publication leaves much to be desired.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHANNES P. MONDT whose telephone number is (571)272-1919. The examiner can normally be reached on 7:30 - 17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Johannes P Mondt/
Primary Examiner, Art Unit 3663